REMARKS

This paper is responsive to the Office action dated October 24, 2002, having a shortened statutory period expiring January 24, 2003, wherein:

Claims 1-39 were previously pending in the application; and

Claims 1-39 were rejected.

No claims have been amended, added, or cancelled by the current amendment. Accordingly, claims 1-39 remain currently pending in the present application.

Rejection of Claims under 35 U.S.C. § 103

In the present Office Action, Claims 1-3 and 22-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.K. Patent No. 2,308,895, issued to Kawashima et al. (hereinafter, "***Kawashima***") in view of U.S. Patent No. 5,513,073, issued to Block et al. (hereinafter, "***Block***"). While not conceding that either of the Examiner's cited references qualify as prior art, but instead to expedite prosecution, Applicants have chosen to traverse the Examiner's rejections as follows. The following arguments are made without prejudice to Applicants' right to establish, for example in a continuing application, that one or more of the Examiner's cited references do not qualify as prior art with respect to an invention embodiment currently or subsequently claimed.

Applicants respectfully submit that neither ***Kawashima*** nor ***Block***, alone or in combination, teaches, shows, or suggests, "a printed circuit board assembly for high-speed optical format data transmission including:

> . . . a heatsink attached to the printed circuit board *wherein the heatsink interfaces with a plurality of the electrical and optical components*,

as required by Applicants' claims (Applicants' claim 1) and further that a *prima facie* case of obviousness under 35 U.S.C. §103 has not been established.

Regarding Applicants' claim 1, the present Office Action states that ***Kawashima*** discloses "a heatsink **30** for dissipating heat, attached to the printed board wherein the heatsink interface with the electrical and optical components" where waveguide **12** and optical wave guide substrate **14** are optical components and transistor **18** is an electrical

component. Applicants respectfully disagree. Referring to **Figure 6** and pages 9-10, ***Kawashima*** teaches that,

> The optical waveguide substrate 14 with its waveguides [**12**]...is mounted on an electronic circuit substrate **24**...that also carries the resistors and other electronic components...optical wave guide substrate **14** is mounted in a depression **25** in the upper side of electronic circuit substrate **24**. A spacer **28** is attached by an adhesive to the lower surface of the electronic circuit substrate **24**...finned heat sink **30** and supporter **32** are attached to the spacer **28**.

Thus, even accepting for the sake of argument the characterization of waveguide **12**, optical wave guide substrate **14**, and transistor **18** as optical and electrical components, ***Kawashima*** neither teaches nor suggests a heatsink which interfaces with a plurality of electrical and optical components. Rather, as clearly shown above, ***Kawashima*** teaches a heat sink **30** attached to a spacer **28**. Applicants further respectfully submit that ***Block*** is not cited for and does not teach, show, or suggest, a heatsink which interfaces with a plurality of electrical and optical components.

Additionally, no attempt has been made to justify the combination of ***Kawashima*** and ***Block*** and thus a *prima facie* case of obviousness has not been established. In addition to the claim elements not taught or suggested by the cited references as described above, the Examiner has not shown any suggestion or motivation to combine ***Kawashima*** and ***Block***, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

Accordingly, Applicants respectfully submit that the rejection of claims 1-3 and 22-23 under 35 U.S.C. 103(a) is improper and further that claim 1 is allowable over ***Kawashima*** and ***Block*** alone or in combination. Applicants' claims 2-9 depend from claim 1 and are allowable for at least those reason(s) stated for the allowability of claim 1. Applicants' claim 22 and corresponding dependent claims 23-30 include one or more limitations substantially similar to those described with respect to Applicants' claim 1 and are therefore allowable for at least those reason(s) stated for the allowability of claim 1.

In the present Office Action, claims 4-39 were rejected under 35 U.S.C. 103(a) as being unpatentable over ***Kawashima*** in view of ***Block*** and further in view of U.S. Patent No. 5,182,632, issued to Bechtel et al. (hereinafter, "***Bechtel***"). While not conceding that the Examiner's cited reference ***Bechtel*** qualifies as prior art, but instead to expedite prosecution, Applicants have chosen to traverse the Examiner's rejections as follows. The following arguments are made without prejudice to Applicants' right to establish, for example in a continuing application, that one or more of the Examiner's cited references do not qualify as prior art with respect to an invention embodiment currently or subsequently claimed.

Applicants respectfully submit that the cited references fail to teach, show, or, suggest all elements of Applicants' claims and further that a *prima facie* case of obviousness under 35 U.S.C. §103 has not been established.

Regarding claims 4 and 24, the present Office Action states that "Bechtel's device discloses the heatsink 104) with an opening to embed electrical or electronic components." Applicants respectfully disagree and traverse as follows.

Applicants respectfully submit that ***Bechtel*** fails to teach, show, or suggest a heatsink including "one or more openings in which one or more of the electrical or optical components are embedded" as required by Applicants' claim. 4 and generally required by Applicants' claim 24. Rather, ***Bechtel*** teaches with respect to heatsink 104 that,

> Attached to the upper surface 104A of heatsink 104 are a plurality, in this case four, of integrated circuit chips 110A, 110B, 110C, and 110D. Interconnect structure 114 fits onto heatsink 104 such that apertures 116 surround each of the integrated circuit chips 110A through 110D...Integrated circuit chips 110A, 110B, 110C, 110D, (see also FIG. 3A), are bonded in spaced positions, by suitable heat conductive adhesive means 112 (see FIG. 3C)...to the inwardly-facing surface 104A of heatsink 104. Thus each chip 110A, 110B, etc. sits in an aperture 116 in interconnect structure 114. (***Bechtel***, Column 6, Lines 15-35, emphasis supplied, see also ***Bechtel***, Fig 3A)

As has been clearly shown, chips **110A**, **110B**, **110C**, and **110D** are bonded onto the surface of heatsink **104** rather than being embedded through one or more openings. Furthermore apertures **116**, taught by ***Bechtel***, are included not within heatsink **104** but

within interconnect structure **114** which Applicants have previously submitted and maintain is not a heatsink and not part of heatsink **104**. Accordingly, Applicants respectfully submit that claims 4 and 24 are independently allowable over ***Kawashima***, ***Block***, and/or ***Bechtel*** alone or in combination.

Regarding claims 10-21, Applicants respectfully submit that ***Kawashima***, ***Block***, and ***Bechtel*** taken alone or in combination fail to teach, show, or suggest a method for dissipating heat from electrical components and optical components on a printed circuit board, comprising

> . . . attaching a heatsink member to the printed circuit board so that the heatsink member is in contact with at least a portion of each electrical and optical component that requires cooling,

as required by Applicants' claim 10 and generally required by Applicants' claim 16. As shown herein, none of the cited references teach, show, or suggest a heatsink in contact with at least a portion of each electrical and optical component that requires cooling. Accordingly, Applicants respectfully submit that claims 10 and 16 are allowable over ***Kawashima***, ***Block***, and/or ***Bechtel*** alone or in combination.

Regarding claims 31-39, Applicants respectfully submit that claim 31 is allowable over ***Kawashima*** and ***Block*** as described above with respect to Applicants' claim 1 and further that ***Bechtel*** is not cited for and does not teach, show, or suggest a heatsink which interfaces with a plurality of electrical and optical components. Accordingly, Applicants respectfully submit that claim 31 is allowable over ***Kawashima***, ***Block***, and/or ***Bechtel*** alone or in combination.

Additionally, no attempt has been made to justify the combination of ***Kawashima***, ***Block***, and/or ***Bechtel*** and thus a *prima facie* case of obviousness under 35 U.S.C. §103 has not been established. In addition to the claim elements not taught or suggested by the cited references as described above, the Examiner has not shown that there is any suggestion or motivation to combine ***Kawashima***, ***Block***, and/or ***Bechtel***, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

Applicants' claims 11-15 depend from claim 10 and are therefore allowable for at least those reason(s) stated for the allowability of claim 10. Applicants' claims 17-21 depend from claim 16 and are therefore allowable for at least those reason(s) stated for the allowability of claim 16. Applicants' claims 32-39 depend from claim 31 and are therefore allowable for at least those reason(s) stated for the allowability of claim 31.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Box Non-Fee Amendment, Commissioner for Patents, Washington, D.C. 20231, on January 24, 2003.

Attorney for Applicant(s) — Date of Signature: 1-24-03

Respectfully submitted,

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